**Course Title: Digital Logic and System Design**

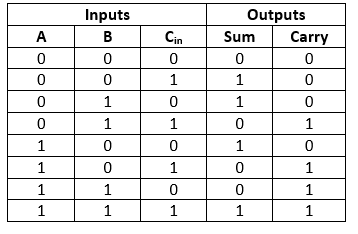
**Course Code: CSE 210**

**Credit Hour: 1.5**

**Experiment No. 2**

**Experiment Name:**

1. **Design the logic circuits from the given Truth table:**



**b) Simplify the given logic expression and verify the truth table.**

**i) (A + C) (A D + A D’) + A C + C**

**ii) A’ B C + A B’ C + A B C’ + A B C (Using K-map)**

**Report:**

1) Problem Statement

2) Instruments (used in this experiment)

3) Simplification of the equation.

4) Circuit Diagram of the equations (both simplified and not simplified)

**i) (A + C) (A D + A D’) + A C + C**

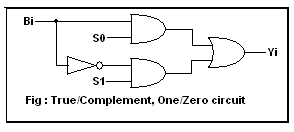
5) Truth table of the equations (both simplified and not simplified)

(i) Y =

|  |  |  |  |
| --- | --- | --- | --- |
| A | B | C | Y |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

6) Discussion mark: 15

Additional work for lab 2:



1. Write the logic expression for above circuit.
2. Construct the truth table and verify it.